anisotropically etching the first and second dielectric regions through the respective first and second openings to create first and second gate trenches;

isotropically etching the first and second dielectric regions in the first and second gate trenches to remove the first and second sidewall portions;

thermally forming a gate oxide on each of the first and second sidewalls of the mesa following the isotropic etching of the first and second dielectric regions; and

forming first and second gate members in the first and second gate trenches, respectively, the first and second gate members comprising polysilicon and being respectively insulated from the first and second sidewalk by the gate oxide.

2. The method of claim **1** further comprising forming first and second field plate members in the first and second trenches, respectively, the first and second field plate members being insulated from the mesa by the first and second dielectric regions, respectively.

3. The method of claim **1** wherein the distance is approximately 0.2 μm to 0.5 μm.

4. The method of claim **1** wherein the distance is greater than a worst-case misalignment of the masking layer.

5. The method of claim **1** further comprising forming a body region near a top surface of the mesa adjacent the first and second gate members, the body region being of a second conductivity type.

6. The method of claim **5** further comprising forming a source region of the first conductivity type at the top surface of the mesa, the source region being disposed above the body region.

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